REMARKS

Reconsideration of the present application is respectfully requested.

The Examiner has stated that Applicant's election of claims 21-37 without traverse is acknowledged. This is incorrect. Applicant asserts that the Response to Restriction Requirement filed on December 28, 2001 clearly indicates Applicant's election of claims 1-20, 38 and 39 without traverse. (Applicant has canceled non-elected claims 21-37 without prejudice in the present Amendment.) Acknowledgement by the Examiner of this election for the record is respectfully requested.

Claim 11 has been objected to due to a noted informality. In response, Applicant has amended claim 11, as well as amended claims 1-6, 8-11, 13, 14, 16-20, 38 and 39 only to correct typing errors and to improve readability thereof.

Claims 1, 2 and 7 have been rejected under 35 U.S.C. §102(b) in view of Kinzer (U.S. 5,644,148). For reasons that will now be discussed, these claims are allowable over the references cited by the Examiner.

In general, there is a need to increase the capacity of electric current in integrated IGBT or DMOS chips. This can be done by increasing the chip area. However, increasing the chip area increases waste and reduces yield when a defect occurs. The claimed invention provides a way of salvaging chips that include defects.

Specifically, independent claim 1 recites that the gate electrodes of one cell block are electrically independent of the gate electrodes of the other cell blocks. Therefore, it can be determined whether each of the cell blocks is defective or not by connecting only gate pads of non-defective cell blocks with a gate terminal provided outside of the semiconductor substrate (page 3 lines 22-26 in the specification of the present invention).

Kinzer discloses in FIG. 2 that a semiconductor substrate (20), a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes (G) respectively provided in the plurality of cell blocks, and a gate pad are provided on the semiconductor substrate and connected with the plurality of gate electrodes. However, Kinzer fails to disclose cell blocks that have corresponding gate pads, as claimed in all the independent claims of the present invention. That is, in column 6, lines 42-47 of Kinzer states as follows:

> The gate segments 31, 32 and 33 will be connected to an appropriate common gate pad (not shown). For purposes of illustration, a gate electrode "G" is shown connected to segment 3, it being understood that this gate electrode will be connected to all of the gate segments of the entire gate mesh.

Therefore, Kinzer discloses a common gate electrode connected to all gates and fails to disclose cell blocks that each have a gate pad. Referring specifically to the language of claim 1, Kinzer fails to show gate electrodes of one cell block that are electrically independent of those of other cell blocks. Therefore, as Kinzer does not anticipate claim 1, and therefore claims 3 and 7 that depend therefrom, Applicant respectfully requests that rejection be withdrawn.

Claims 3 and 16-19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Smith (U.S. 6,329,692) and Kohno (U.S. 6,180,966). This rejection is respectfully traversed.

Amended claims 3 and 17-19 recite that the non-defective first cell block is connected with a gate terminal and a defective second cell block is connected with a ground terminal. Therefore, a gate controlling signal is not fed to the gate electrode of the defective cell block so that elements in the defective cell block are not operated.

Smith discloses in FIG. 4 that a gate of the transistor 42 connects with a ground terminal Vss via resistor 44, and a gate of the transistor 36 connects with a gate terminal VDD. However, the transistor 36 must be formed by a non- defective cell and should be appropriately operated as part an electric circuit shown in FIG. 4.

Kohno discloses in FIG. 2 a plurality of cell blocks in which the over current can damage the cells. However, the defective portion existing where a cell is formed is basically formed during the substrate formation process, and thus represents a different type of the damage caused by over current flowing in the cells.

Accordingly, neither Kinzer, Smith nor Kohno discloses a plurality of cell blocks where gate electrodes of one cell block are independent from those of other cell blocks. This feature is important for disabling defective cell blocks without having to discard the entire chip when a defect is present. Thus, even if Smith or Kohno was combined with Kinzer, the terms of the claims would still not be taught or suggested by the prior art combination.

Claim 5 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Sanchez (U.S. 6,160,305). This rejection is respectfully traversed.

Sanchez discloses in FIG. 1 that a gate of a transistor 20 connects with an output terminal and a gate of the transistor 16 connects with an emitter terminal of the transistor 12 to create an emitter potential. However, the transistor 16 must be formed by a non- defective cell and should be appropriately operated as part of an electric circuit shown in FIG. 5. Thus, even if Sanchez was combined with Kinzer, the terms of the claims are not taught or suggested by the prior art combination as the same reason as discussed in connection with claims 3 and 16-19.

Claims 8-15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Calhoun (U.S. 4,631,569). This rejection is respectfully traversed.

Amended claim 8 recites that a plurality of marks is respectively provided on the cell blocks to distinguish whether each of the cell blocks is defective. Therefore, it can be easily determined via the marks whether the gate pads are connected with the non-defective cell block or the defective cell block. Accordingly, the gate pads connected with the non-defective and defective cell blocks can be respectively connected with different terminals.

Calhoun discloses plurality of circuit cells in which the defective cells are marked to be distinguished from the working cells. However, again, Calhoun fails to disclose a plurality of cell blocks where gate electrodes of one cell block are independent from those of other cell blocks. Thus, even if Calhoun was combined with Kinzer, the terms of the claims would not be taught or suggested by the combination.

Claim 20 has been rejected §103(a) as being unpatentable over Kinzer in view of Smith, Kohno and Calhoun (U.S. 5,793,065). This rejection is respectfully traversed.

Amended claim 20 recites that the plurality of cell blocks includes a first group of cell blocks, which have an equal threshold voltage and are connected with the gate terminal, and a second group of cell blocks, which have different threshold voltages from one another and are connected with one of the plurality of pads. That is, the first group of non-defective cell blocks is connected with the gate terminal, while the second group of defective cell blocks is connected with the pads with an emitter potential. Therefore, elements in the non-defective cell block are operated and elements in the defective cell block are not operated.

Shinohe discloses that the use of adjacent elements having different threshold voltages reduces the adverse influence of threshold voltage differences among the elements. However, in such a configuration, the different threshold voltages are intentionally formed to reduce the adverse influence. This feature is different from that recited in claim 20. Further, Shinohe fails to disclose a plurality of cell blocks where gate electrodes of one cell block are independent from

those of other cell blocks. Therefore, Shinohe fails to cure the shortcomings of Kinzer, Smith, and Kohno. Thus, even if these references were combined, the terms of the claims would not be satisfied by the combination.

Claims 38 and 39 have been rejected §103(a) as being unpatentable over Kinzer in view of Smith and Crane (U.S. 6,339,191). This rejection is respectfully traversed.

Regarding amended claims 38 and 39, these claims are different from Kinzer as mentioned above. Crane discloses trays for carrying dies. However, Crane fails to disclose a plurality of cell blocks where gate electrodes of one cell block are independent from those of other cell blocks. Therefore, even if Smith and Crane were combined with Kinzer, the terms of the claims would not be satisfied by the prior art combination.

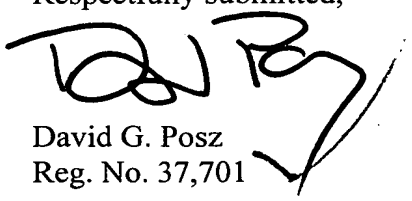
As for new claims 40-51, independent claim 40 recites a plurality of transistor cells that are divided into groups. The groups of claim 40 are the same as the cell blocks of claim 1. Claim 40 also recites a plurality of common gate electrodes for the groups, respectively. The word "respectively" indicates that each group has a separate common gate electrode. This feature is not shown by any of the prior art references of record as indicated in the discussion of the rejected claims above.

Accordingly, Applicant respectfully requests the examiner's §102(b) rejection of claim 1 and §103 rejection of claims 3, 8,17-20, 38 and 39 be withdrawn, and that the Examiner allow new claims 40-51. Further as the claims 2, 5, 6, 7 and 9-16 depend from the aforementioned claims, they are allowable for the same reasons as amended claims 1, 3, 5, 6 and 17-20.

In view of the above amendments and remarks, the present application is now believed to be in condition for allowance. A prompt notice to that effect is respectfully requested.

A petition for 1-month extension of time is enclosed. Please change any additional unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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MARKED UP VERSION OF AMENDED CLAIMS

Please amend claims 1-6, 8-11, 13, 14, 16-20, 38 and 39

as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of cell blocks provided on the semiconductor substrate, wherein each cell block includes a plurality of transistor cells;

a plurality of gate electrodes [electrically independent of one another and respectively provided in the plurality of cell blocks] formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block are electrically independent of the plurality of gate electrodes of other cell blocks; and

a plurality of gate pads provided on the semiconductor substrate [and respectively connected with the plurality of gate electrodes] corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to one of the plurality of gate electrodes of the corresponding cell block.

2. (Amended) The semiconductor device according to claim 1, wherein:

the semiconductor substrate has a rectangular shape; and

the plurality of gate pads are arranged [at a side portion] along a side of the semiconductor substrate.

3. (Once Amended) The semiconductor device according to claim 1, further comprising:

a ground terminal provided outside of the semiconductor substrate [and grounded]; and

a gate terminal provided outside of the semiconductor substrate [and] , the gate terminal being electrically independent of the ground terminal, wherein:

the plurality of cell blocks includes a first non-defective cell block [that is non-defective,] and a second defective cell block [that is defective]; and

the plurality of gate pads includes a first gate pad [connecting] that connects the first non-defective cell block to the gate terminal, and a second gate pad [connecting] that connects the second defective cell block to the ground terminal.

4. (Amended) The semiconductor device according to claim 3, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is [boned] bonded to the ground terminal by one of wire-bonding, soldering, and pressure-welding.

5. (Amended) The semiconductor device according to claim 1, further comprising:

a gate terminal provided outside of the semiconductor substrate;

[an emitter pad provided on the semiconductor substrate to have an emitter potential;]

a source or emitter pad provided on the semiconductor substrate [to have] , wherein the source or emitter pad has a source potential or an emitter potential, wherein:

the plurality of cell blocks includes a first non-defective cell block [that is non-defective,] and a second defective cell block [that is defective]; and

the plurality of gate pads includes a first gate pad [connecting] that connects the first non-defective cell block to the gate terminal, and a second gate pad [connecting] that connects the second defective cell block to [one of] the emitter or source pad [and the source pad].

6. (Amended) The semiconductor device according to claim [4] 5, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is bonded to the [one of the emitter] source or emitter pad [and the source pad] by one of wire-bonding, soldering, and pressure-welding.

8. (Amended) The semiconductor device according to claim 1, further comprising a plurality of marks provided at a plurality of regions of the semiconductor substrate, wherein the plurality of marks respectively [corresponding] corresponds to the plurality of cell blocks, each of the plurality of marks being for discriminating whether a corresponding [one of the cell blocks] cell block is defective.

9. (Amended) The semiconductor device according to claim 8, wherein discrimination of whether each of the plurality of cell blocks is defective is determined by

at least one of [a] location, [a] color, [a] size, and [a] shape of a corresponding one of the plurality of marks [on the semiconductor substrate].

10. (Amended) The semiconductor device according to claim 8, wherein discrimination of whether each of the plurality of cell blocks is defective is determined by a number of the plurality of marks corresponding to [the] each of the plurality of cell blocks.

11. (Amended) The semiconductor device according to claim 8, wherein:

the plurality of cell blocks [include] includes a first cell block;

the plurality of [gat] gate pads [include] includes a first gate pad connected with the first cell block; and

the plurality of marks includes a first mark for discriminating whether the first cell block is defective, the first mark being provided on a line passing through the first gate pad.

13. (Amended) The semiconductor device according to claim 11, wherein:

the plurality of cell blocks [include] includes a second cell block;

the plurality of gate pads [include] includes a second gate pad connected with the second cell block;

the plurality of marks [include] includes a second mark for discriminating whether the second cell block is defective, the second mark being [provided out of] located apart from a line passing through a center of the second gate pad[;

first one of the first cell block and the second cell block is defective; and

second one of the first cell block and the second cell block is non-defective].

14. (Amended) The semiconductor device according to claim 8, wherein[,] each of the plurality of marks is [provided is at a vicinal region] <u>located in a vicinity</u> of a corresponding gate pad or on a surface of the corresponding gate pad.

16. (Amended) The semiconductor device according to claim 1, further comprising a plurality of pads having an emitter potential and provided on the semiconductor substrate [adjacently] <u>adjacent</u> to the plurality of gate pads.

17. (Amended) The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor substrate, wherein:

the plurality of cell blocks includes a first cell block and a second cell block, the first cell block being non-defective and connected with the gate terminal[,] <u>and</u> the second cell block being defective and connected with one of the plurality of pads <u>having an emitter potential</u>.

18. (Amended) The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided in the plurality of cell [block] <u>blocks</u>;

a plurality of emitter pads provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes;

a collector electrode provided on a back surface of the semiconductor substrate;

an emitter terminal bonded to the main surface of the semiconductor substrate and electrically connected with the plurality of emitter pads;

a collector terminal bonded to the back surface of the semiconductor substrate and electrically connected with the collector electrode; and

a resin member encapsulating the gate terminal, the emitter terminal, and the collector terminal together.

19. (Amended) The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided in the plurality of cell blocks;

a plurality of emitter pads [electrodes] provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes; and

an emitter terminal provided outside of the semiconductor substrate and electrically connected with the emitter pads, wherein:

the first cell block is connected to the gate pad through a first bonding wire; and

the second cell block is connected to the one of the plurality of pads through a second bonding wire.

20. (Amended) The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor device, wherein:

the plurality of cell blocks includes a first group of cell blocks [having] , which have an equal threshold voltage and are connected with the gate terminal, and a second group of cell blocks [having] , which have different threshold voltages from one another and are connected with one of the plurality of pads.

38. (Amended) An apparatus for manufacturing an insulated gate type power IC, comprising:

a chip transfer machine including a plurality of trays for selectively holding a plurality of chips, [each of which] wherein each chip includes: [has a semiconductor substrate, a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes respectively provided on the cell blocks and electrically independent of one another, and a plurality of gate pads respectively connected with the gate electrodes, wherein:]

a semiconductor substrate;

a plurality of cell blocks on the substrate, wherein each cell block includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block is electrically independent of the plurality of gate electrodes of others of the plurality of cell blocks; and

a plurality of gate pads on the substrate and respectively corresponding to the plurality of cell blocks, wherein each gate pad is connected to the plurality of gate electrodes of a corresponding cell block; wherein:

the plurality of chips [being] is sorted based on an arrangement position of a defective cell block of each [cell] chip [to be selectively held by] in one of the plurality of trays;

the defective cell block has a corresponding gate pad that is connected with one of a ground terminal having a ground potential and an emitter pad having an emitter potential; and

a non-defective cell block of each [cell] of the plurality of chips has a corresponding gate pad that is connected with a gate terminal provided outside of the semiconductor substrate.

39. (Amended) An insulated gate type power IC module [, comprising] that includes a plurality of insulated gate type ICs, each of the [plurality of] insulated gate type ICs comprising:

a semiconductor substrate;

[a plurality of cell blocks provided on the semiconductor substrate;

a plurality of gate electrodes respectively provided in the plurality of cell blocks and electrically independent of one another; and

a plurality of gate pads respectively connected with the plurality of gate electrodes, wherein:]

a plurality of cell blocks located on the substrate, each of which includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the cell blocks, wherein the plurality of gate electrodes of one cell block is electrically independent of the plurality of gate electrodes of others of the plurality of cell blocks; and

a plurality of gate pads on the substrate corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to the plurality of gate electrodes of a corresponding cell block; wherein:

each of the insulated gate type ICs includes a defective cell block at an identical position[,] and a non-defective cell block, the defective cell block having a corresponding gate electrode that is connected with one of a ground terminal provided outside of the semiconductor substrate and an emitter pad provided on the semiconductor substrate, the non-defective cell block having a corresponding gate electrode that is connected with a gate terminal provided outside of the semiconductor substrate; and

the insulated gate type power IC module is composed exclusively of the plurality of insulated gate type ICs [exclusively].